Remarks

Claims 1-17 are pending in the present application. Claims 1-17 stand rejected under 35 U.S.C. 102(b) and 103(a) as being anticipated and obvious over Fujimoto. In view of the following remarks, reconsideration and withdrawal of these grounds of rejection is requested.

Claim Rejections Under 35 U.S.C. § 112

Claim 6 is rejected under 35 U.S.C. § 112, Second Paragraph, as being "indefinite." Particularly, the Examiner contends that it is not clear how "at least one transistor" can comprise a "number of transistors." Applicant hereby amends dependent claim 6 to specify that the "at least one transistor" recited in claim 1 comprises a "specific number of transistors selected to provide an optimum noise characteristic." It is a well-established tenet of claim interpretation that the modifier "at least one..." means 'one or more' of the specified element. Accordingly, reconsideration and withdrawal of this ground of rejection is respectfully requested.

Claim Rejections Under 35 U.S.C. § 102

Claims 1-16 are rejected under 35 U.S.C. § 102(b) as being anticipated by Fujimoto et al. (U.S. Pat. No. 5,809,408). For the reasons set forth in detail below, reconsideration and withdrawal of this ground of rejection is respectfully requested.

Claim 1 recites:

> A multi-stage amplifier comprising: a first amplifier stage including at least one first transistor, said at least one first transistor selected to provide an optimum noise characteristic; and, a second amplifier stage including at least one second transistor,

> said at least one second transistor selected to provide an optimum gain characteristic. [emphasis added].

Thus, claim 1 requires a multi-stage amplifier including a "first stage" with an amplifier selected to provide an "optimum noise characteristic", and a "second stage" with an amplifier selected to provide an "optimum gain characteristic." As discussed below, Fujimoto fails to disclose, teach or suggest such an invention.

Fujimoto teaches a variable gain circuit which includes plural gain stage blocks 20A-20N (See Fig. 3). Each gain stage block 20A-20N includes three amplifiers, an input amplifier A_{in}[#], a middle amplifier A[#], and an output amplifier A_{out} [#] (e.g., amplifiers 21a, 22a and 23a in gain stage block 20A). All the "A_{in}" input amplifiers (i.e., 21a, 21b, etc.) are selected to have identical input impedances. Similarly, all the "A_{out}" output amplifiers (i.e., 23a, 23b, etc.) are selected to have identical output impedances (see, col. 4, line 64 to col. 5, line 7).

Fujimoto does not disclose, teach or suggest a multi-stage amplifier including at least one transistor selected to provide an "optimum noise characteristic" and at least one transistor selected to provide an "optimum gain characteristic." At best, Fujimoto teaches selecting amplifiers to provide identical input and output impedances in a multi-stage device. Hence, reconsideration and withdrawal of this ground of rejection with respect to claim 1, and claims 2-9 dependent thereon, is respectfully requested.

Independent claim 10 recites similar limitations to those discussed above with reference to independent claim 1. In particular, claim 10 recites a method whereby transistors are selected based on "optimum noise" and "optimum gain" characteristics. Accordingly, for those reasons discussed above with reference to independent claim 1, reconsideration and withdrawal of this rejection with respect to claims 10-16 is also respectfully requested.

Claim Rejections Under 35 U.S.C. § 103

Claim 17 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Fujimoto et al. For the reasons set forth in detail below, reconsideration and withdrawal of this ground of rejection is respectfully requested.

Independent claim 17 recites similar limitations to those discussed above with reference to independent claim 1. In particular, claim 17 recites a method whereby transistors are selected based on "optimum noise" and "optimum gain" characteristics. Accordingly, for those reasons discussed above with reference to independent claim 1, reconsideration and withdrawal of this rejection with respect to claim 17 is also respectfully requested.

Conclusion

In view of the foregoing remarks, Applicants submit that this application is in condition for allowance at an early date, which action is earnestly solicited.

Respectfully submitted,

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